

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

5. (Previously Presented): A comparison circuit for an analog/digital converter comprising:

a network of comparators each comparing an analog voltage to be converted with a reference voltage (Vref), the reference voltages being distributed over a range in which the analog voltage can vary, each comparator comprising a direct output and an inverse output, wherein each output, direct or inverse, is linked to the input of a voltage follower, the outputs of each voltage follower being connected either to inputs of a first network of resistors delivering at its outputs, mean voltages that are the average of those present on direct outputs of the comparators receiving reference voltages similar in their distribution over the range, or to inputs of a second network of resistors delivering at its outputs, mean voltages that are the averages of those present on inverse outputs of comparators receiving reference voltages similar in their distribution over the range.

6. (Previously Presented) The comparison circuit as claimed in Claim 5, wherein the outputs of the first network of resistors are connected, by way of voltage followers, to inputs of a third network of resistors delivering at its outputs, mean voltages that are the averages of those present on neighboring inputs of the third network of resistors, and wherein the outputs of the second network of resistors are connected, by way of voltage followers, to inputs of a fourth network of resistors delivering at its outputs, mean voltages that are the averages of those present on neighboring inputs of the fourth network of resistors.

7. (Previously Presented) The comparison circuit as claimed in claim 5, wherein the networks of resistors have the same structure.

8. (Currently Amended) The comparison circuit as claimed in Claim 7, wherein each network of resistors comprises a first series assembly of two identical pairs of two identical resistors in series, ~~on-the-one-hand, on-the-other-hand,~~ and a second series assembly of two identical pairs of two identical resistors in series ~~on-the-one-hand, on-the-other-hand~~ and wherein the inputs of the network of resistors are constituted by the ends and the midpoint of the first series assembly, and the outputs of the network of resistors are constituted by the ends and the midpoint of the second series assembly, the midpoint of the first pair and of the second pair of resistors of the first assembly are connected respectively to the midpoint of the first pair and of the second pair of the second assembly.